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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/726,391	12/01/2000	Edward Colles Nevill	550-189	1282

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NIXON & VANDERHYE, PC
1100 N GLEBE ROAD
8TH FLOOR
ARLINGTON, VA 22201-4714

EXAMINER	
BULLOCK JR, LEWIS ALEXANDER	
ART UNIT	**PAPER NUMBER**
2127	

DATE MAILED: 11/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/726,391	NEVILL, EDWARD COLLES	
	Examiner	Art Unit	
	Lewis A. Bullock, Jr.	2127	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/13/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

Article 1 denoted as , H. Stone, Chapter 12 – "A Pipeline Push-Down Stack Computer", 1969, pgs. 235-249 cannot be considered because the copy is too dark to be considered. Applicant is requested to resubmit a copy of the cited reference.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 and 7-14 are rejected under 35 U.S.C. 102(e) as being anticipated by BAK (US 6,513,156).

As to claim 1, BAK teaches an apparatus (computer system) for processing data, the apparatus comprising: a processor core (central processor); a main memory (system memory) operable to store instruction words and data words (col. 4, line 58 – col. 5, line 20); a data store (bytecode table / management information section of snippet) operable to store words from the main memory accessed by a data store port of the processor core (col. 12, lines 53 – col. 13, line 30); an instruction store (instruction section of snippet zone / template table) operable to store words from the

main memory accessed by an instruction store port of the processor core (col. 8, lines 11-42; col. 12, lines 53 – col. 13, line 30); and an instruction interpreter (interpreter / virtual machine) operable to read instruction words from the instruction store (col. 5, lines 31-61; col. 6, line 61 – col. 7, line 11); wherein the instruction interpreter (interpreter / virtual machine) is operable to modify a slow form instruction (original virtual machine instruction) within the instruction store to a fast form instruction (new virtual machine instruction / native form instruction considered a higher level bytecode) and to write the fast form instruction to the data store (via overwriting the original virtual machine instruction with the new virtual machine instruction) (col. 7, lines 12-67; col. 9, lines 6-62), the slow form instruction and the fast form instruction having a common functionality when executed by the interpreter (executes the same function); and the instruction interpreter (interpreter / virtual machine) is operable upon reading a slow form instruction (virtual machine instruction) from the instruction store to check for a corresponding fast form instruction (new virtual machine instruction / native instruction that considered a higher level bytecode) within the data store and if the fast form instruction is present within the data store, then to execute the fast form instruction instead of the slow form instruction (col. 7, lines 12-67; col. 8, lines 1-58; col. 6, lines 45-50; col. 7, lines 54-62; col.8, lines 32-35).

As to claim 7, BAK teaches the slow form instruction results in an unresolved storage access request to one or more stored words (via the amount of execution time to load the values or next instruction for execution) and the fast form instruction (native

form instruction that is considered a higher level bytecode) results in a resolved storage access request to the one or more stored words (via referencing the information already stored) (col. 6, lines 5-50; col. 6, lines 45-50).

As to claim 8, BAK teaches the slow form instruction (original virtual machine instructions) includes a symbolic reference to a required element (loop instructions) (col. 8, line 59 – col. 9, line 5) and the fast form instruction (new virtual machine instruction / native form instruction that is considered a higher level bytecode) includes a numeric reference to the required element (index to snippet) (col. 8, lines 11-26, lines 43-58; col. 6, lines 45-50).

As to claim 9, BAK teaches the slow form instruction (typical java bytecodes) invokes an additional data processing procedure before completion (compilation into bytecodes and then being interpreted) (col. 5, lines 13-20).

As to claim 10, BAK teaches the slow form instruction and the fast form instructions are Java Virtual Machine Instructions ("Conceptually, therefore a snippet may be considered as an implementation of a higher level bytecode that implements the operations of a sequence of lower level bytecodes.") (col. 5, lines 13-20; col. 7, lines 28-53; col. 6, lines 45-50).

As to claim 11, BAK teaches the slow form instructions are getstatic, putstatic or invoke (col. 8, line 59 – col. 9, line 5).

As to claim 12, BAK teaches the fast form instruction is invokenonvirtual_quick (go-native instruction / native form instruction that conceptually represents a higher level bytecode) (col. 8, lines 1-58; col. 6, lines 45-50).

As to claim 13, BAK teaches the instruction interpreter (interpreter / virtual machine) translates Java Virtual Machine instructions to native instructions of the processor core (col. 6, line 31 – col. 7, line 67).

As to claim 14, reference is made to a method that corresponds to the apparatus of claim 1 and is therefore met by the rejection of claim 1 above.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over BAK (US 6,513,156).

As to claims 2-4, BAK teaches an instruction interpreter for translating and interpreting the instructions (col. 5, lines 31-61; col. 6, line 61 – col. 7, line 11). However, BAK, does not mention whether the interpreter is hardware-based, software-based, or a combination of both. Official Notice is taken in that it is well known in the art that an interpreter is implemented as a hardware interpreter, a software interpreter, or a combination of both and therefore would be obvious to one skilled in the art that the interpreter is one of a software interpreter, a hardware interpreter, or a combination of both in order to interpret the instructions.

As to claims 5-6, BAK teaches the data store and instruction store is used by the system in determining whether there exist and to use a fast form instruction (new virtual machine instruction / native instruction representing of a higher level bytecode) (col. 12, lines 53 – col. 13, line 30; col. 7, lines 12-67; col. 8, lines 1-58; col. 9, lines 6-62; col. 6, lines 45-50). It is inherent within the teachings that the stores reside in system memory. BAK also teaches that the computer system includes more than one processor or a cache memory (col. 5, lines 1-2). However, BAK does not teach that the stores are maintained in a data cache. Official Notice is taken in that it is well known to one of ordinary skill in the art that the stores may reside on the cache for quick access.

Response to Arguments

5. Applicant's arguments filed 7/7/04 have been fully considered but they are not persuasive. Applicant argues that Bak does not disclose that upon reading an original

virtual machine instruction (selected for replacement), the instruction interpreter checks for a corresponding go-native (fast-form) instruction in the bytecode table and then executes the go-native instruction instead of the original virtual machine instruction. The examiner disagrees. First, the fast form instructions are not limited to just the new virtual instructions that replaces the original virtual instruction to be replaced, but is also considered to be the native form instructions. Bak teaches that upon a virtual machine instruction of a function being interpreted for execution, a determination is made whether this is a new or original form instruction. If the instruction is a new instruction then the native form instruction resident in the snippet zone is invoked for execution, otherwise well known techniques for executing a virtual instruction is performed. This determination of whether the instruction is a new or original instruction is the check. Therefore, the cited teachings of Bak teaches performing a check for a correspond gonative instruction instead of the original virtual machine instruction. Secondly, the independent claims do not teach that the fast form instruction is a go-native instruction or that the slow form instructions are virtual machine instructions. The claims at best teaches that the interpreter upon reading a slow form instruction, i.e. an instruction that is slower than another instruction, from the instruction store to check for a corresponding fast form instruction, i.e. an instruction that is faster than another instruction, within the data store and, if the fast form instruction is present within the data store, then to execute the fast form instruction instead of the slow form instruction. As detailed above, Bak teaches this limitation. Dependent claims 10-13 teaches that the slow and fast form instructions are virtual machine instructions. In examining these

claims, the examiner makes reference to Bak wherein the embodiment has the advantange of increasing the execution speed of Java virtual machine instructions and is not limited to any particular language, computer architecture, and specific implementation. Furthermore, Bak teaches that a snippet is conceptually an implementation of a higher level bytecode that implements the operations of a sequence of lower level bytecodes (col. 6, lines 45-50). Therefore, Bak teaches the generation of fast form virtual machine instructions (instructions stored in a snippet) from slow form virtual machine instructions (original virtual machine instructions).

Applicant then argues that Bak does not teach that the data store and the instruction store is operable to store words from main memory and is accessed by a processor core. The examiner disagrees. Bak teaches the system comprises a cabinent which houses a CD-ROM drive, system memory and a hard drive which may be utilized to store and retrieve software programs incorporating computer code that implements the invention, data for use with the invention, and the like (col. 4, lines 46-50). Bak further teaches that although CDROM is shown, other computer readable storage media including floppy disk, tape, flash memory, system memory, and hard drive may be utilized (col. 4, lines 51-54). Bak teaches that a computer program is stored in memory and accessed by a virtual machine in order to interpret and execute the program by using snippets which store not only the new native instructions but also data relating to the overwritten instructions, which are stored separately from the program. Therefore, Bak teaches a plurality of memory stores, i.e. main memory, data store, and instruction stores, that store words from a main memory that stores the

original program and accessible by a processor core, i.e. virtual machine. Therefore, the examiner believes the claims are met by the teachings of Bak and maintains the rejection.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lewis A. Bullock, Jr. whose telephone number is (571) 272-3759. The examiner can normally be reached on Monday-Friday, 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LEWIS A. BULLOCK, JR.
PRIMARY EXAMINER

November 10, 2004